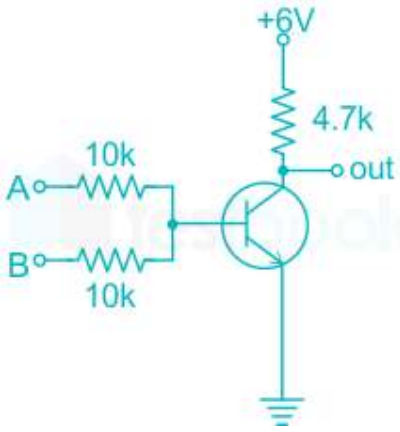
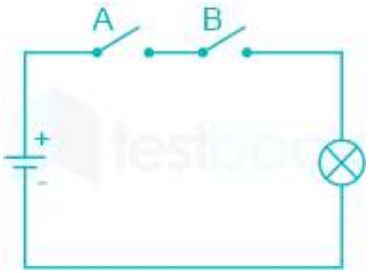
Boolean Algebra & Logic gates MCQ Objective Questions:

1. The following circuit behaves as a:



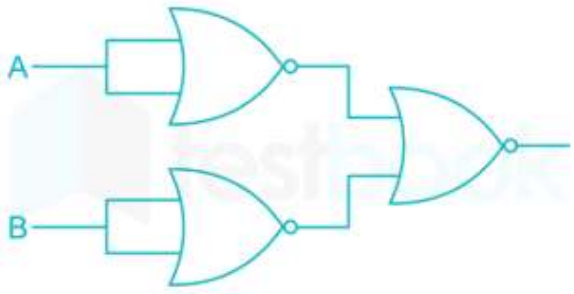
a) AND Gate b) NAND Gate c) OR Gate **d) NOR Gate**

2. Which logic gate is represented by following circuit?



a) AND Gate b) NAND Gate c) NOT Gate **d) OR Gate**

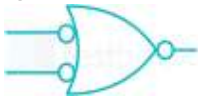
3. The logic function implemented in the following figure is:

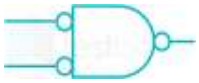


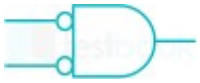
a) AND Gate b) NAND Gate c) NOT Gate d) OR Gate

4. The symbol for two - input OR- gate in negative logic is:

a) 

b) 

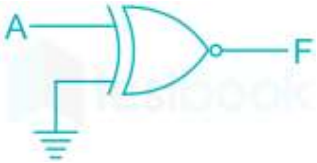
c) 

d) 

5. The following gates are designated as Universal Gates

a) NOT, OR and AND b) XOR, OR and AND c) XNOR, NOR and NAND **d) NOR and NAND**

6. The output of the logic gate in figure is

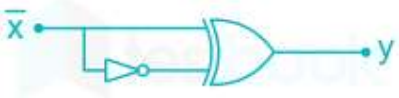


a) 0 b) 1 **c) A'** d) A

7. The minimum number of 2-input NAND gates required to implement a 2-input XOR gate is

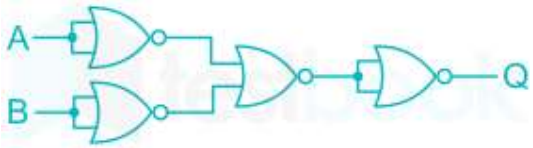
a) 3 b) 5 c) 6 **d) 4**

8. The output Y of the logic circuit given below is:



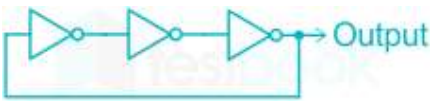
a) **1** b) 0 c) X d) X'

9. The output of logic circuit given below represents _____ gate.



a) OR b) NOR **c) NAND** d) AND

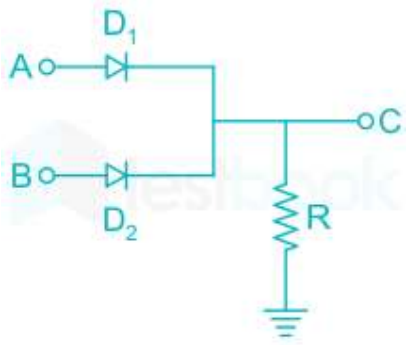
10. What will be the fundamental frequency for the following circuit if each inverter delay is 100 nsec?



a) 1GHz b) 0.5GHz c) 3.34MHz **d) 1.67MHz**

11. The minimum number of NAND gates required to realize AB + AB'C + AB'C' is
    a) 3 b) 2 c) 1 **d) 0**

12. Which of the following logical operations could be computed by the given network?



a) C = AB **b) C = A + B** c) C= (A.B)' d) C=(A+B)'

13. Which of following logic gates provides output as 0 when both inputs are same (either 0 or 1)?

    a) XNOR **b) XOR** c) NOR d) NAND

14. Who invented Boolean algebra?
a) Bardeen b) Claude Shannon **c) George Boole** d) None of the above

15. _____ are the methods used to represent negative integer numbers.

    a) 1's compliment b) Sign magnitude c) 2's compliment **d) All of the above**

16. How many types of number systems are there?
    a) One b)Two c) Three d) Four

17. The base is 16 for _____ number system
    a) Binary **b) Hexadecimal** c) Decimal d) Octal

18. The American standard code for information interchange has _____ characters
    a) 64 b) 25 **c) 128** d) None of the above

19. What is the standard form of ECDIC?
    a) Extended Binary Coded Decimal Interchange Code
    b) Extended Binary Coded hexadecimal Interchange Code
    c) Extended Binary Coded Decimal Information Code
    d) None of the above

20. How many types of parities are there?
    a) One **b) Two** c) Three d) Four

21. The ones complement of binary number 1010 is _____
    a) 0101 b) 1010 c) 0110 d) 1110

22. The 2's complement of binary number 1010 is _____
    a) 0101 b) 1010 **c) 0110** d) 1110

23. The base is eight for _____ number system
    a) Binary b) Hexadecimal c) Decimal **d) Octal**

24. IC's are categorized into _____

a) One **b) Two** c) Three d) Four

(Linear & digital)

25. How many gates does ultra large-scale integration contain?
    a) 100 gates b) 1000 gates c) 10000 gates **d) More than 100,000 gates**

26. How many gates does large-scale integration contain?
    a) **100 to 10,000 gates** b)10,000 to 100,000 gates
    b) 10000 gates d) None of the above

27. The base is ten for _____ number system
    a) Binary b) Hexadecimal c) Decimal d) Octal

28. What are the advantages of ICs?
    a) Small in size b) Low-cost c) Operating speed is high **d) All of the above**

29. Which IC is a quad two-input NAND gate?
    a) 74LS00 b) 74LS01 c) 74LS03 **d) All of the above**

30. The supply voltage of the 7400 series TTL family IC's is _____
    a) 1V b) 2V c) 4V **d) 5V**

31. What is the standard form of TTL?
    a) Transistor-Transistor Logic b) Transistor Transducer Logic
    b) Transducer Transistor Logic d) None of the above

32. The voltage range of low power Schottky is _____
    a) 1V b) 2V c) 4V **d) 5V**

33. The maximum toggle speed of the 7400 TTL family ICs is _____
    a) 20MHz b) 10 MHz c) 15 MHz **d) 25 MHz**

34. The speed of the low power Schottky is _____
    a) 2ns b) 8ns **c) 10ns** d) 12ns

35. The power of the low power Schottky is _____
    a) 1mW **b) 2mW** c) 4mW d) None of the above

36. The voltage range of advanced low power Schottky is _____
    a) 1V b) 2V c) 4V **d) 5V**

37. The speed of the advanced low power Schottky is _____
    a) 2ns **b) 7ns** c) 10ns d) 12ns

38. The power of the advanced low power Schottky is _____
    a) 1mW b) 2mW c) 4mW d) None of the above

39. The maximum input current of the silicon gate CMOS is _____
    a) 0.1mA b) 0.5mA **c) ±0.0001mA** d) None of the above

40. The maximum clock of silicon gate CMOS is _____
    a) 20MHz **b) 40 MHz** c) 15 MHz d) 25 MHz

41. The propagation time delay of the silicon gate CMOS is _____
    a) 2ns b) 7ns c) 10ns **d) 8ns**

42. Which IC is quad two-input AND gate?
    a) 74LS08 b) 74LS00 c) 74LS01 d) All of the above

43. The maximum input current of the metal gate CMOS is _____
    a) 0.0001mA **b) -0.0001mA** c) ±0.0001mA d) None of the above

44. The maximum clock of the metal gate CMOS is _____
a) 20MHz b) 40 MHz **c) 12 MHz** d)25 MHz

45. The propagation delay of the metal gate CMOS is _____
    a) 2ns b) 7ns c) 10ns **d) 105ns**

46. How many types of logic families are there?
    a) Two b) Four c) Six **d) Seven**

47. What is the standard form of IIL?
    a) Injection Integrated Logic **b) Integrated Injection Logic**
    b) Integrated Integrated Logic d)None of the above

48. The noise immunity is excellent in _____ logic family
    a) CMOS b) TTL c) ECL d) None of the above

49. The maximum input current of the Schottky TTL gates is _____
    a) -2.0mA b) 2.0mA c) -2.5mA d) -1.0mA

50. The maximum clock of low power Schottky TTL is _____
    a) 20MHz **b) 40 MHz** c) 12 MHz d) 25 MHz

51. The propagation delay of the low power Schottky TTL is _____
    a) 2ns b) 7ns **c) 10ns** d)105ns

52. The fanout of the CMOS logic family is _____
    a) >10 b) >20 c) >30 **d) >50**

53. What are the components used in the RTL logic family?
    a) Resistors b) Transistors **c) Both a and b** d) None of the above

54. The TTL family is classified into _____
    a) Two **b) Four** c) Six d) Seven

55. Which IC is a quad two-input NOR gate?
    a) 74LS02 b) 74LS01 c) 74LS00 d) None of the above

56. The maximum input current of the low power Schottky TTL is _____
    a) 0.2mA b) 0.3mA **c) -0.4mA** d) 0.1mA

57. The maximum clock of Schottky TTL gate is _____
    a) 20MHz b) 40 MHz c) 12 MHz **d) 125 MHz**

58. **The fan-out of TTL logic family is _____**
    a) 2 b) 5 c) 8 **d) 10**

59. The fan-out of the ECL logic family is _____
    c) 10 b) 20 **c) 25** d) None of the above

60. What are the components used in the ECL logic family?
    a) Resistors b) Transistors **c) Both a and b** d) None of the above

61. In which logic family the power dissipation is very low?
    a) RTL b) DCTL **c) CMOS** d) TTL

62. Which one belongs to the unipolar logic family?
    a) RTL, DCTL, DTL b) TTL, ECL **c) CMOS, PMOS, NMOS** d) None of the above

63. The noise margin in TTL logic family is _____
    a) Moderate b) Low c) High d) None of the above

64. The noise immunity of the CMOS logic family is _____
    a) Poor b) Good **c) Very strong** d) Strong

65. _____ are the delay of the signal transition from input to output
    a) Propagation delay b) Threshold voltage

    c) Power dissipation d) None of the above

66._____ is the multiplication of propagation delay and power dissipation

a) Propagation delay b) Threshold voltage c) Power dissipation **d) Figure of merit**